

Automatic Optimizations for Runtime Verification Specifications

JAN BAUMEISTER, CISPA Helmholtz Center for Information Security, Germany

BERND FINKBEINER, CISPA Helmholtz Center for Information Security, Germany

MATTHIS KRUSE, Saarland University, Germany

STEFAN OSWALD, CISPA Helmholtz Center for Information Security, Germany

NOEMI PASSING, CISPA Helmholtz Center for Information Security, Germany

MAXIMILIAN SCHWENGER, CISPA Helmholtz Center for Information Security, Germany

Automatically transforming program code to yield binaries optimized for execution speed is a heavily researched topic. Research on program transformations mainly focuses on conventional, imperative programming languages. Formal specification languages are easier to analyze due to their formal core, restrictiveness and freedom of side effects. This talk reports on recent work on how to best make use of these properties, exemplified on the stream-based runtime monitoring specification language RTLOLA. Since a specification is part of a safety-critical component, it should not forsake legibility for efficiency. At the same time, if the monitor will be deployed on an embedded system, reducing its resource footprint is essential. To this end, the RTLOLA framework employs transformations on several levels when synthesizing executable code from a specification. The first set of transformations work on an intermediate representation of the specification itself. The second one concerns code generation for high-level monitor code, and lastly the compilation of the high-level code into an executable employs conventional compiler transformations.

Additional Key Words and Phrases: Runtime Verification, Stream Monitoring, Specification Languages

Runtime monitors are deployed to increase the safety of and confidence into a cyber-physical system. If the monitor is synthesized from a formal specification, the process has to satisfy two major criteria. First, the underlying specification has to be legible, which reduces the chance of specification errors and improves understandability for third parties. Secondly, the resulting monitor needs to be able to operate in the low-resource environment of an embedded system.

Legibility and performance are often contrary, so it is desirable to transform a legible specification into a performant one automatically. Simple and naive solutions tend to be easiest to grasp and hence perfect in a safety-critical context. However, they often consume more memory or require more processing power than strictly necessary. A solution is to apply automatic transformations to a legible specification, leaving the semantics provably intact while benefiting the performance of the resulting monitor.

In this talk, we are going to report on how recent work employs this idea in the RTLOLA framework. In a nutshell, the framework synthesizes an executable monitor for a given specification. The underlying eponymous stream-based specification language contains information on how to refine incoming data, *input streams*, into output streams. It also contains criteria for when the refined data indicates a potentially unsafe situation. The synthesis of the executable monitor is a multi-step process as outlined in Figure 1. Here, each step can be subject to performance-enhancing transformations.

The first step is the transformation of a linear specification into a tree-like intermediate representation (IR). Transformations enhancing the IR are particularly effective as they have an immediate effect on any further steps. Hence,

This work was partially supported by the German Research Foundation (DFG) as part of the Collaborative Research Center Foundations of Perspicuous Software Systems (TRR 248, 389792660), by the European Research Council (ERC) Grant OSARES (No. 683300), and by the Aviation Research Programm LuFo of the German Federal Ministry for Economic Affairs and Energy as part of "Volocopter Sicherheits-Technologie zur robusten eVTOL Flugzustands-Absicherung durch formales Monitoring" (No. 20Q1963C).

