

# FPGA Stream-Monitoring of Real-time Properties

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## ABSTRACT

An essential part of cyber-physical systems is the online evaluation of real-time data streams. Especially in systems that are intrinsically safety-critical, a dedicated monitoring component inspecting data streams to detect problems at runtime greatly increases the confidence in a safe execution. Such a monitor needs to be based on a specification language capable of expressing complex, high-level properties using only the accessible low-level signals. Moreover, tight constraints on computational resources exacerbate the requirements on the monitor. Thus, several existing approaches to monitoring are not applicable due to their dependence on an operating system.

We present an FPGA-based monitoring approach by compiling an RTLOLA specification into synthesizable VHDL code. RTLOLA is a stream-based specification language capable of expressing complex real-time properties while providing an upper bound on the execution time and memory requirements. The statically determined memory bound allows for a compilation to an FPGA with a fixed size. An advantage of FPGAs is a simple integration process in existing systems and superb executing time. The compilation results in a highly parallel implementation thanks to the modular nature of RTLOLA specifications. This further increases the maximal event rate the monitor can handle.

## KEYWORDS

Stream Specification Languages, Real-time Properties, Runtime Verification, FPGA

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## 1 INTRODUCTION

With the growing autonomy of cyber-physical systems, the evaluation, aggregation, and monitoring of real-time data have become essential for ensuring the safety of the system. A principled approach to building such monitors is provided by stream-based specification languages like RTLOLA [17, 18]. Input streams that collect data from sensors, networks, etc., are filtered and combined into output streams that contain data aggregated from multiple sources and over multiple points in time such as over sliding windows of some real-time length. Trigger conditions over these output streams then identify critical situations.

Previous work has been very successful in using stream-based specifications for analyzing recorded data streams, such as the flight data of drones [1, 17] and network traces [16]. However, tools that have been developed for the offline analysis of recorded data cannot directly be used for online monitoring, such as for an onboard monitoring component on a drone. The reason is the substantial software overhead of such offline tools. Cyber-physical systems operate under narrow constraints on the available resources. A monitor must, specifically, process all data in real time and within the available memory.

In this paper, we present a compilation approach that realizes RTLOLA specifications on field-programmable gate arrays (FPGAs). FPGAs have dramatic advantages over software-based solutions in terms of processing speed due to the inherent parallelism, and also in terms of other factors such as energy consumption, weight, and ease of integration within the cyber-physical system.

In RTLOLA, input streams are event-driven, i.e., without a priori known frequencies; output streams are typically periodic. This difference is reflected in the realization of the monitor as a two-module architecture consisting of a high-level controller and a low-level controller. The role of the high-level controller is to receive the events, prepare stream evaluations and to schedule periodic tasks. The low-level controller then computes new stream values based on the information received from the high-level controller and triggers an alarm when appropriate.

A key challenge for the compilation is the treatment of sliding window expressions. In general, there is no bound on the memory needed to store the potentially unbounded number of events received during the time period of the window. Our monitoring circuit splits the full window into smaller chunks, where the data

can be pre-aggregated without loss of precision. As a result, the number of registers needed for the monitor can (under some mild assumptions on the aggregation functions) be determined statically.

The immediate compilation to a hardware description language allows us to achieve a high level of parallelism. For this, we analyze the specification to identify modular sub-structures and evaluate them in parallel. We showcase the impact of this analysis with a synthetic case study. Furthermore, we demonstrate the practicality of the compilation by presenting experimental data from two realistic case studies from avionics and network monitoring. Both case studies indicate that the compilation utilizes the benefits of hardware: the implementation is highly efficient, requires only a small board, and consumes less than 2 W of power.

The main contribution of this paper is an automatic compilation of an RTLOLA specification into an FPGA monitor. The resulting circuits have a clear structure following the formal RTLOLA semantics. The monitor is decoupled from the observed system. Unlike instrumentation-based approaches [10, 13], the monitor is independent of the origin of the data. Furthermore, there are no assumptions on the frequency of the inputs granted it is lower than the maximum clock frequency of the FPGA.

The monitor utilizes the inherently parallel nature of hardware: the high-level controller is organized into a pipeline architecture, which ensures that new events can enter the controller before the processing of the previous events has been completed. In the low-level controller, the evaluation order ensures that independent streams are processed in parallel. Moreover, the monitor is highly space and energy efficient. Unlike interpreter-based approaches [10, 12], which include a general-purpose runtime environment, the compiled circuit is strictly limited to the operations that actually occur in the specification. The monitors of our case studies run, as a result, on small FPGA boards with little power (< 2 W).

## 1.1 Related Work

Most of the earlier work on formal runtime monitoring was based on temporal logics [15, 20, 23, 26, 27, 38]. The approaches vary between inline methods that realize a formal specification as assertions added to the code to be monitored [23], or outline approaches that separate the implementation of the monitor from the one of the system under investigation [20]. Based on these approaches and with the rise of real-time temporal logics such as MTL [25] and STL [31], a series of works introduced monitoring algorithms for real-time properties [2, 3, 14, 36].

First translations from temporal logics to monitoring circuits have been introduced with the tools FoCs [11], developed at IBM Haifa, P2V [30], a compiler that translates assertions written in sPSL [8] to Verilog code, BusMOP [37], which synthesized monitor circuits from specifications written in past-time linear temporal logic for monitoring PCI bus traffic, and MBAC [6], an automata-based monitor synthesizer for PSL properties. Inspired by these constructions, an optimized approach for bounded future properties was presented in [19]. Hardware runtime monitors for real-time properties were presented by Jaksic et al. [24], where monitors for STL specifications were implemented in an FPGA. Further work on FPGA implementations of real-time temporal specification was

introduced with the tool R2U2 [34, 35], an outline monitoring approach that allows for monitoring specifications in MTL including future-time specifications.

Temporal logics come with the advantage of providing formal guarantees on the space and time complexity of the synthesized monitors. However, a major drawback of these logics is their expressiveness. When monitoring cyber-physical systems, one needs to express properties beyond yes and no verdicts (for example with some degree of arithmetic operation) to be able to monitor realistic properties of the system. Stream-based languages over complex datatypes like RTLOLA [17, 18] provide such expressiveness and further maintain a desirable level of formal guarantees.

The stream-based approach to monitoring was pioneered by the specification language LOLA [12]. LOLA is related to synchronous programming languages like Lustre [7, 22], and Esterel [5], which have been widely used for the development of digital circuits [4]. In contrast to these languages, LOLA is a descriptive language, which subsumes the temporal logics and can express both past and future properties. A feature of LOLA is that upper bounds on the memory required for monitoring can be computed statically. RTLOLA extends LOLA with asynchronous streams and real-time features such as sliding windows. Two other extensions of LOLA are TeSSLa and Striver. TeSSLa [10] allows for monitoring piece-wise constant signals where streams can emit events at different speeds with arbitrary latencies. It relies on the instrumentation of C code and is thus not independent of the monitored system. Moreover, RTLOLA comes with the feature of computing aggregations over sliding windows, and allows for the decoupling of the computation of output streams from variable input event rates via fixed-rate clocks. The main difference between RTLOLA and Striver [21] is that RTLOLA has both variable-rate and fixed-rate streams and provides convenient, native operators such as sample-and-hold and sliding windows that translate between the two types of streams. The fixed rate in RTLOLA allows for a more direct translation to a hardware implementation of the monitor.

An approach for compiling synchronous LOLA has been presented in [32]. We remove the assumption of synchronously arriving data and add real-time capabilities to the specification language.

## 2 RTLOLA

RTLOLA [18] is a *stream-based* specification language with real-time features based on the specification language LOLA [12]. In stream-based runtime monitoring, sensor readings are interpreted as streams of input data. These streams are fed into a stream engine that computes new sequences of data called output streams based on the values of input streams. The output streams compute statistics over the sensor data and allow for stating verdicts about the monitored system. The computation rules for output streams are defined in RTLOLA by a stream equation, which is a defining equation that maps a stream variable to a stream expression. Consider for example a GPS module in a drone that delivers data about the current longitude and latitude, and a monitor that checks if the GPS module is delivering data in appropriate frequencies. An RTLOLA specification for defining such a monitor is given by the following stream definitions:

```

input gps: (Float64, Float64)
output gps_glitch: Bool@1Hz :=
  gps.aggregate(over:2s, using:count) < 10
trigger gps_glitch "GPS sensor frequency < 5Hz"

```

The stream `gps` is an input stream that represents the readings of the GPS module and is expected to deliver data with a frequency greater than or equal to 5 Hz. To check whether this data is delivered with the expected frequency, we define the output stream `gps_glitch` that computes a sliding window with a duration of two seconds over the stream `gps`. The stream `gps_glitch` is computed in a frequency of 1 Hz and checks whether ten values are received from the GPS module in the last two seconds. The window over the input stream `gps` is computed via the expression `gps.aggregate(over:2s, using:count)`, which counts the number of data values of `gps` in the last two seconds. If the number of values is less than 10, then `gps_glitch` evaluates to true. In this case, an alarm is raised with the message "GPS sensor frequency < 5Hz". This alarm is defined by the trigger expression `trigger gps_glitch`.

The stream above is a *periodic* stream and as such computed at a fixed frequency. In addition to that, RTLOLA also allows for the definition of *event-based* streams by omitting the frequency. Event-based streams are evaluated whenever streams occurring in its stream expression are evaluated. For example, if we want to check whether a vehicle is slowing down, we can compute the change in velocity between the last two velocity sensor readings:

```

input velo: Float64
output slowing_down: Bool :=
  velo - velo.offset(by:-1).defaults(to:0) < 0

```

The stream `slowing_down` is computed every time `velo` receives a new value. To compute the difference, the stream expression uses the *offset operator* to access the last (`.offset(by:-1)`) and current value of the stream `velo` and then compute the difference between these two values. In case the value of an offset operation is not defined, the default operator (`.defaults(to:d)`) returns the value `d`. In the example above, `velo.offset(by:-1)` is not defined before receiving the first velocity reading, so the default value 0 is used instead.

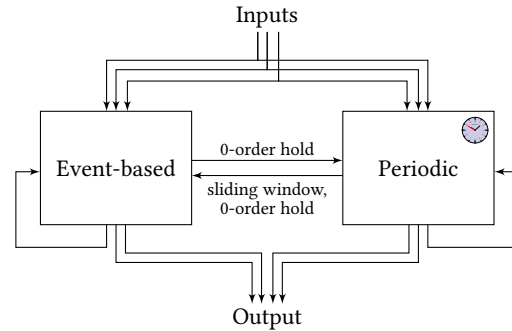
In the case where an output stream is defined over more than one stream, the output stream is evaluated only if all streams it depends on are evaluated as well. If one of these values is missing, one can still enforce the computation of the stream using the *sample-and-hold operator* (`.hold()`). This operator accesses the last value computed for a stream. If it is not present, the provided default operator (`.defaults(to:d)`) is used. The following specification clarifies the role of this operator.

```

input gps: (Float64, Float64)
input height: Float64
output too_low: Bool := if zone(gps)
  then (height.hold().defaults(to:300)) < 300
  else false
trigger too_low "Flying low in inhabited area"

```

The function `zone` determines whether the drone is in an inhabited area. When the vehicle is in this area, the specification checks whether its current height (`height`) is less than 300 feet. If this is



**Figure 1: Stream accesses of event-based and periodic streams in RTLOLA**

the case, an alarm is raised because it violates the flight regulations for inhabited areas.

RTLOLA imposes some rules on how streams may access the values of other streams. Figure 1 shows the general picture of RTLOLA specifications. The values of an output stream may be used in the definitions of other output streams as long as the following rules are respected:

*Access via sliding window:* Periodic streams may access values of other streams via a sliding window without any further restriction.

*Access via offset operator:* When accessing a stream with the offset operator, an RTLOLA specification must respect the following rules:

1. *Accessing periodic streams in event-based streams:* These accesses are only allowed with the sample-and-hold operator.
2. *Accessing event-based streams in event-based streams:* These accesses are always valid. However, the accessing stream is only extended if all accessed streams are extended at the same time. The sample and hold operation eliminates this dependency.
3. *Accessing event-based streams in periodic streams:* Periodic streams only access event-based streams with the sample-and-hold operator.
4. *Accessing periodic streams in periodic streams:* A periodic stream  $s$  may access the values of another periodic stream  $s'$  if and only if the frequency of  $s'$  is an integer-multiple of the one of  $s$ . Otherwise the access is only allowed via the sample-and-hold operator.
5. *Recursive stream access:* Any stream is allowed to access its own history of values as long as it does not create any circular access like accessing itself with an offset of 0. Consider the following specification:

```

output num_glitches: UInt32 :=
  num_glitches.offset(by:-1).defaults(to:0) +
  (if gps_glitch then 1 else 0)

```

The output stream is an event-based stream that is evaluated every time a new value is computed for `gps_glitch`. Note that there is no need for the sample-and-hold operator as the output stream only depend on `gps_glitch`. If the new value of `gps_glitch` is true, then the new value of `num_glitches` is computed by increasing its last value (`num_glitches.offset(by:-1).defaults(to:0)`) by one. Otherwise, if `gps_glitch` is false, the new value of `num_glitches` is equal to its last one.

For the full syntax and type system of RTLola we refer the reader to the technical report<sup>1</sup> [18].

In the rest of the paper we use the variables  $n^\uparrow$ ,  $n^\downarrow$  and  $n^*$  to indicate the number of output streams, number of input streams and number of triggers in an RTLola specification, respectively.

## 2.1 Monitoring RTLola Specifications

Monitoring an RTLola specification consists of receiving events, evaluating stream expressions, and triggering alerts when necessary. The separation of event-based and periodic streams manifests itself in the monitoring algorithm in that it consists of an event-based and a periodic process.

The event-based process receives an event and extends streams according to the *evaluation order*  $<$ , i.e., if the stream expression of stream  $s$  contains a lookup with target  $s'$ , then  $s' < s$ . Thus,  $s'$  needs to be extended before  $s$ . The event-based process respects this by successively evaluating streams as soon as the evaluation order permits it.

The periodic process schedules streams according to their frequency. Since all frequencies are determined a priori, we can compute an array of *deadlines*, where deadline  $D_i$  is a delay  $d_i$  and a set of streams  $S_i$  such that when  $D_{i-1}$  was due, after  $d_i$  seconds,  $S_i$  need to be evaluated. The least common multiple of the periods of all periodic streams is the *hyper-period*  $\Pi$  and  $\#dl$  denotes the number of deadlines within one hyper-period. Like the event-based process, the periodic process also respects the evaluation order.

An RTLola specification can be monitored in one of two modes. Offline mode describes a monitoring process that happens after the fact based on log data. It is useful for post-mortem analyses or for validating a specification based on previous system runs. Online mode, however, is the concurrent execution of a system and its monitor. FPGA-based monitoring is especially interesting for the online mode because this mode requires timely processing of events and imposes tighter restrictions on the monitor in terms of available resources.

The major difference between the two modes in the evaluation process is the source of the current timestamp. In online mode, the value is the system time of the monitor. In offline mode, however, events are annotated with time stamps. The monitor considers the received time stamp to be the current time and checks whether a deadline would have been missed. If so, it first computes all periodic streams affected by the deadline. Afterwards, it processes the event as described before.

## 2.2 Sliding Windows

The evaluation of sliding windows needs special attention. Assume the stream expression of  $s$  with frequency  $x\text{Hz}$  contains a sliding window expression such as  $s'.\text{aggregate}(\text{over}:\delta, \text{using}:\gamma)$  for some duration  $\delta$  and aggregation function  $\gamma$ . A naive implementation requires to store all values of  $s'$  within the last  $\delta$ s, which is unfeasible because there is no information about the arrival frequency of  $s'$ . If  $\gamma: A^* \rightarrow B$  is a *list homomorphism* as defined by Maarten [33], the sliding window can be evaluated accurately with only a finite amount of memory. List homomorphisms can be

<sup>1</sup>The technical report also describes parametrization with dynamic stream creation, which we do not consider here.

Event	Time	velo	$p_1$	$p_2$	$p_3$	avg_velo
	0.0 s		$\epsilon$	$\epsilon$	$\epsilon$	
1	0.5 s	10.0	$\epsilon$	$\epsilon$	(10.0,1)	
2	0.6 s	10.1	$\epsilon$	$\epsilon$	(20.1,2)	
	1.0 s		$\epsilon$	$\epsilon$	(20.1,2)	8.0
	2.0 s		$\epsilon$	(20.1,2)	$\epsilon$	8.0
3	2.2 s	9.9	(20.1,2)	$\epsilon$	(9.9,1)	
	3.0 s		(20.1,2)	$\epsilon$	(9.9,1)	10.0

Figure 2: Detailed computation of a sliding average.

split into four components: a unary map:  $A \rightarrow T$  and finalization  $\text{fin}: T \rightarrow B$ , an associative binary reduction  $\oplus: T \times T \rightarrow T$ , and a neutral element  $\epsilon$  w.r.t.  $\oplus$ . Assuming  $\gamma$  is a list homomorphism, we utilize the fact that sliding windows only occur in periodic streams. All new values occurring within a  $x$ s time interval are effectively equivalent w.r.t. their arrival time. We now apply the *bucketing* approach proposed by Li et al. [28] and split the duration of the window into  $\delta x^{-1}$  equal-sized buckets. Each bucket stores an intermediate value, initialized with  $\epsilon$ , and pre-aggregates all values within two evaluations of the window expression using  $\oplus$ . At the time of the evaluation, the intermediate values get reduced to obtain the final value.

Fortunately, many commonly used aggregation functions are list homomorphisms, such as summation, minimization, maximization, counting, integration, and averaging.

As an example, consider the following specification:

```
input velo : Float32
output avg_velo @1Hz :=
  velo.aggregate(over: 3s, using: avg)
  .defaults(to: 8.0)
```

Since the average is a list homomorphism, we define the following concrete components:

- $\text{map}: \mathbb{R} \rightarrow \mathbb{R} \times \mathbb{N}$  with  $\text{map}(v) := (v, 1)$
- $\text{fin}: \mathbb{R} \times \mathbb{N} \rightarrow \mathbb{R}$  with  $\text{fin}(v, c) := \frac{v}{c}$
- $\oplus: (\mathbb{R} \times \mathbb{N})^2 \rightarrow \mathbb{R} \times \mathbb{N}$  with  $(v_1, c_1) \oplus (v_2, c_2) := (v_1 + v_2, c_1 + c_2)$
- $\epsilon := (0, 0)$

Figure 2 details the computation of the average with three buckets. We list the values for all buckets at points in time when either an event arrives or `avg_velo` gets computed. Here,  $p_1$  represents the “oldest” bucket, and  $p_3$  the most recent one.

Initially, all buckets contain the element  $\epsilon$ . Upon receiving the first velocity at time stamp 0.5 s, the value of the last bucket is changed to  $(0, 0) \oplus \text{map}(10.0) = (10.0, 1)$ . When the next event is received at time stamp 0.6 s, we add the value to the same bucket and get  $(10.0, 1) \oplus \text{map}(10.1) = (20.1, 1)$ . At time stamp 1.0 s, we compute `avg_velo` for the first time. Since the current time stamp is less than the length of the window, the default values is used. Afterwards, we evict the oldest bucket, shift all bucket values to the left, and add a new one with value  $\epsilon$ . The same happens at time stamp 2.0 s. The next event arrives at time stamp 2.2 s and is added to  $b_3$ . At time 3 s, we stop using the default value and aggregate the buckets. The resulting value is finalized, i.e.,  $\text{fin}((20.1, 2) \oplus (0, 0) \oplus (9.9, 1)) = \frac{30}{3} = 10$

### 3 COMPILATION

The hardware realization of an RTLOLA specification consists of two modules connected via a first-in-first-out queue as can be seen in Figure 3. The *High-level Controller (HLC)* receives external events consisting of event data for each affected input stream and a time stamp in offline mode, as well as the system time in online mode. The HLC acts as mediator between event-based inputs and periodic deadlines, such that later components in the architecture do not need to distinguish them anymore. The number of bits the HLC receives is  $s_{ts} + \sum_{i=1}^{n^{\downarrow}} (s_i + 1)$  where  $s_{ts}$  and  $s_i$  denote the number of bits required to represent a single timestamp and value of input stream  $i$ , respectively. The additional bit per input stream indicates whether the current event contains a new value for the respective stream. The HLC decides whether a periodic deadline is due or an event ought to be evaluated. This decision is based on information about events and the internal system clock. The respective information is preprocessed with respect to the specification and stored in the *Queue*. It consists of  $s_{ev} = (\sum_{i=1}^{n^{\downarrow}} (s_i + 1)) + s_{ts} + n^{\uparrow}$  bits with the following semantics:

- (1)  $\sum_{i=1}^{n^{\downarrow}} (s_i + 1)$  bits encode an event as explained before. If the signal encodes a deadline, all bits are 0 indicating that no data is available.
- (2)  $s_{ts}$  bits contain the time stamp used for the evaluation of sliding windows and as implicitly defined input stream with name time.
- (3)  $n^{\uparrow}$  bits declare for each output stream whether or not they are affected by the current deadline or event.

The *Low-level Controller (LLC)* uses this information to manage the evaluation process: all input streams, and output streams which expression can be evaluated immediately are extended first, followed by the remaining output streams in further steps according to the evaluation order. The LLC also manages updates and the evaluation of sliding windows occurring in output stream expressions.

Due to the lower complexity of HLC's task, it is capable of receiving events faster than the LLC can process them. For this reason, the queue acts as a buffer between the two components. While this does not prevent a loss of data when the pressure on the evaluator exceeds its limits for an extended amount of time, it temporarily relieves the stress of a sudden burst of events. Moreover, it cleanly decouples the two components, enabling them to work independently and concurrently at their own pace.

#### 3.1 Notation

We first introduce some notation. The  $\circ$  operator denotes bit-concatenation.  $0^n$  denotes an  $n$ -fold concatenation of 0-bits. Let  $x$  be a bit string of length  $n$ .  $x[i]$  denotes the  $i$ th bit of  $x$  assuming  $i < n$ .  $x[\ell \dots u]$  is the substring  $x[\ell] \circ x[\ell + 1] \circ \dots \circ x[u - 1]$  for  $\ell < u < n$ . The bounds can be omitted, i.e.,  $x[\dots u] = x[0 \dots u]$  and  $x[\ell \dots] = x[\ell \dots n]$ . Further, let  $\xi$  be the internal system clock rate and sums over all input streams are abbreviated by omitting the limits, i.e.,  $\sum s_i = \sum_{1 \leq i} s_i$ .

We distinguish between signals and registers. The former are data lines between components, which we will write in a slanted font, such as *signal*. The latter are mere flip-flop components that are updated with a rising clock edge, written in bold face: **register**.

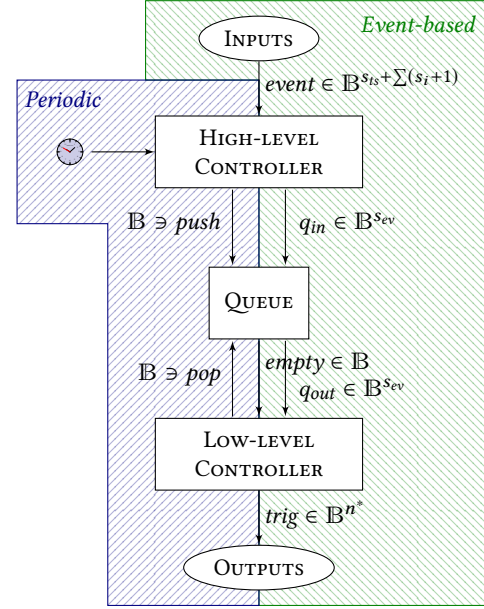


Figure 3: Schematic of an RTLOLA monitor composed of two modules connected via a queue. The *High-level Controller* manages the order in which periodic and event-based streams have to be evaluated. The *Low-level Controller* manages the evaluation process of all affected streams.

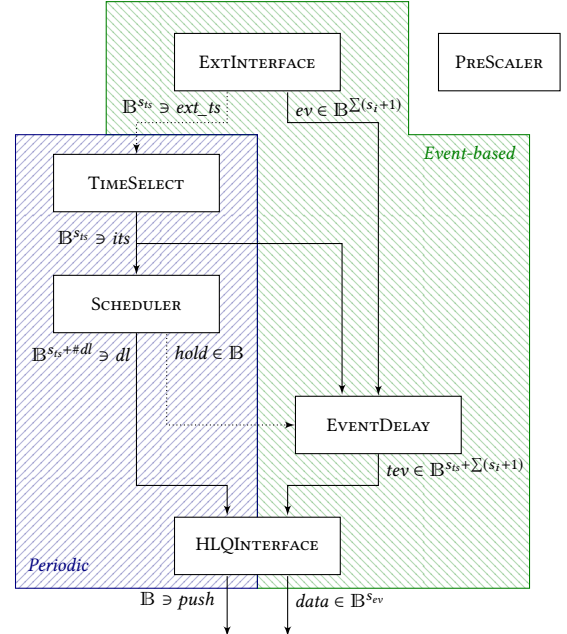


Figure 4: Schematic of the High-level Controller receiving external events, managing periodic deadlines, and preparing data for the Low-level Controller.

### 3.2 High-level Controller

This module receives external events and schedules periodic tasks. It pre-processes data with respect to the specification and stores the information in the queue.

Figure 4 shows the schematic of the module. Dotted lines represent signals and components that are only present in the offline mode. The HLC has access to the common system clock  $sclk$ , and two registers **avail** and **din** which are written by an external entity and contain data of new events. The components are organized in a pipeline architecture, which ensures that new events can enter the controller before the processing of the previous events has been completed. The green, top-left-striped part handles the event-based inputs, whereas the blue, top-right striped part handles periodic deadlines. The HLQINTERFACE then unifies events and deadlines.

**PRESCALER.** This component scales the system clock  $sclk$  down by a constant factor to the HLC-internal  $hclk$  clock.  $hclk$  drives the SCHEDULER, EVENTDELAY, and the EXTINTERFACE. The PRESCALER also provides an internal clock for the HLQINTERFACE, which ticks twice as fast as  $hclk$  and slower than  $sclk$ . For a cleaner illustration, Figure 4 does not include the respective data lines, as well as  $valid$  bits accompanying every data line with width greater than 1 indicating the presence of meaningful data on the wire.

**EXTINTERFACE.** This component handles the communication with external input sources. The external source writes a 1-bit latch **avail** when new input data is available in the **din** register. In online mode, the EXTINTERFACE reads **din**, and forwards it to the EVENTDELAY. In offline mode, the input event also contains a time stamp, which the EXTINTERFACE extracts and forwards to the TIMESELECT component. In both modes, it then clears **avail**, indicating that the next event can be received.

Formally, EXTINTERFACE waits on  $hclk$  and behaves as follows, where  $ev$  carries the event data,  $ext\_ts$  is the external time stamp received with the event, and  $valid\_ext\_ts$  indicates whether there is new and valid data on the  $ext\_ts$  wire.

$$\begin{aligned}
ev^0 &= 0^{\sum s_i} \\
ev^{t+1} &= \begin{cases} \mathbf{din}^t[s_{ts} \dots] & \text{if } \mathbf{avail}^t \\ 0^{\sum s_i} & \text{otherwise} \end{cases} \\
\mathbf{avail}^0 &= 0 \\
\mathbf{avail}^{t+1} &= \begin{cases} 1 & \text{if } external^t \wedge \neg \mathbf{avail}^t \\ 0 & \text{otherwise} \end{cases} \\
ext\_ts^0 &= 0^{s_{ts}} \\
ext\_ts^{t+1} &= \begin{cases} \mathbf{din}^t[\dots s_{ts}] & \text{if } \mathbf{avail}^t \\ 0^{s_{ts}} & \text{otherwise} \end{cases} \\
valid\_ext\_ts^0 &= valid\_ev^0 = 0 \\
valid\_ext\_ts^{t+1} &= valid\_ev^{t+1} = \mathbf{avail}^t
\end{aligned}$$

Here,  $external$  is an oracle indicating a change depending on an external event.

**TIMESELECT.** The component waits on the system clock and computes the internal time stamp  $its$ . In offline mode, this is simply the time stamp formerly extracted from the input event. Thus, this component boils down to a simple wire and does not introduce

any delay in the signal. In online mode, however, this component computes the time that has passed so far by repeatedly adding the period  $\xi$  of the system clock. This component uses an internal register **reg\_its** mirroring the value of  $its$ . It persists the value of the signal without introducing a delay<sup>2</sup>.

$$\begin{aligned}
\mathbf{reg\_its}^0 &= 0^{s_{ts}} \\
\mathbf{reg\_its}^{t+1} &= \mathbf{reg\_its}^t + \xi = (t+1) * \xi \\
its^t &= \mathbf{reg\_its}^t \\
valid\_its^t &= 1
\end{aligned}$$

**SCHEDULER.** This component inspects the current internal time-stamp  $its$  and detects when a periodic stream is due. It first determines the start time and stores it in the **period** register: in online mode that is simply  $0^{s_{ts}}$ , whereas in offline mode this is the first time stamp received from the external source. It then maintains the invariant that **period** contains the least time stamp in the current hyper-period. If, for example, the specification contains two periodic streams with frequency 2 Hz and 5 Hz, then the hyper-period is 1 s. If the first received event carries the timestamp 3.4 s, **period** remains 3.4 s until a time stamp greater than or equal to  $3.4 s + \Pi = 4.4 s$  is received. In this case, it jumps to 4.4 s. As a result, the difference between  $its$  and **period** represents the time within the current hyper-period.

The register **did** contains the id of the current deadline, i.e., the deadline that needs to be evaluated next, in unary encoding. The encoding is a trade-off: a binary encoding requires fewer registers and wires but also two decoders, one in the SCHEDULER and one in the HLQINTERFACE. The **did** register is initialized with  $0^{\#dl}$ , which is an invalid unary number and indicates that the SCHEDULER has not been initialized, i.e., it did not receive a start time, yet. The initialization takes place in the first cycle in online mode, or in the first cycle with enabled  $valid\_ext\_ts$  bit in offline mode.

Lastly, the  $prog(ress)$  signal indicates whether a new deadline is due. It checks whether the SCHEDULER was initialized and whether the position in the current hyper-period exceeds the current deadline. For this check, it accesses the statically determined array of deadline offsets as described in Section 2.1. The lookup consists of conjoining each element of the array with the respective bit of the **did** and bitwise disjoining all results:  $dl(\mathbf{did}) = \bigvee_{i=1}^{\#dl} dl_i \wedge \mathbf{did}[i]$

In the following definitions, a subscript  $off$  ( $on$ ) indicates the offline (online) version of the register or signal. Usages without subscript use the respective version.

$$\begin{aligned}
init_{off}^0 &= 0 \\
init_{off}^{t+1} &= valid\_its^{t+1} \wedge (\mathbf{did}^t = 0^{\#dl}) \\
init_{on}^t &= \begin{cases} 1 & \text{if } t = 1 \\ 0 & \text{otherwise} \end{cases} \\
\mathbf{did}^0 &= 0^{\#dl} \\
\mathbf{did}^{t+1} &= \begin{cases} 10^{\#dl-1} & \text{if } init_{on}^{t+1} \\ csr(\mathbf{did}^t) & \text{if } \neg init_{on}^{t+1} \wedge prog^{t+1} \\ \mathbf{did}^t & \text{otherwise} \end{cases}
\end{aligned}$$

<sup>2</sup>This can be achieved by letting the input wire of the register carry the same signal as the output wire.

$$\begin{aligned}
\text{period}^0 &= 0^{\#dl} \\
\text{period}_{off}^{t+1} &= \begin{cases} its^{t+1} & \text{if } init^{t+1} \\ \text{period}_{off}^t + \Pi & \text{if } \mathbf{did}^t = 0^{\#dl+1} \wedge prog^{t+1} \\ \text{period}_{off}^t & \text{otherwise} \end{cases} \\
\text{period}_{on}^{t+1} &= \begin{cases} 0 & \text{if } init^{t+1} \\ \text{period}_{on}^t + \Pi & \text{if } \mathbf{did}^t = 0^{\#dl+1} \wedge prog^{t+1} \\ \text{period}_{on}^t & \text{otherwise} \end{cases} \\
prog^{t+1} &= \mathbf{did}^t \neq 0^{\#dl} \wedge (its^{t+1} - period^t) > dl(\mathbf{did}^t)
\end{aligned}$$

Here, *csr* is a 1-bit cyclic shift to the right. The output signals are thus defined as:

$$\begin{aligned}
hold_{on}^t &= 0 & hold_{off}^t &= prog^t \\
dl^t &= its^t \circ \mathbf{did}^t & valid\_dl^t &= \neg prog^t
\end{aligned}$$

*EVENTDELAY*. This component composes the internal time stamp and the current event. The time stamp is later used in the evaluation process. In online mode, the compound signal is then passed to the *HLQINTERFACE* without delaying the signal.

In offline mode, however, the *EVENTDELAY* needs to take the *hold* signal into account. To compensate for the delay introduced by the *SCHEDULER*, the compound signal is delayed by one cycle. Afterwards, the data is delayed further until *hold* turns off. During the hold period, new events can be received and need to be stalled. We discuss this issue below.

Formally, the component waits on *hclk* and uses two internal registers, **data** which introduces the mandatory one-cycle delay and **reg\_tev** mirroring the signal *tev*.

$$\begin{aligned}
\mathbf{data}^0 &= 0^{1+s_{ts}+\sum(s_i+1)} \\
\mathbf{data}^{t+1} &= \begin{cases} \mathbf{data}^t & \text{if } hold^{t+1} \\ valid\_ev^{t+1} \circ its^{t+1} \circ ev^{t+1} & \text{otherwise} \end{cases} \\
\mathbf{stalled}^0 &= 0^{1+s_{ts}+\sum(s_i+1)} \\
\mathbf{stalled}^{t+1} &= \begin{cases} \mathbf{stalled}^t & \text{if } hold^{t+1} \\ \mathbf{data}^t & \text{otherwise} \end{cases} \\
tev^t &= \mathbf{stalled}^t[1 \dots] \\
valid\_tev^{t+1} &= \neg hold^{t+1} \wedge tev^t[0]
\end{aligned}$$

Note that *ev* and *its* are always valid at the same point in time, so we can verify the invariant

$$\forall t: valid\_ev^t \iff valid\_its^t$$

*QInterface*. This component accepts data from the *EVENTDELAY* and the *SCHEDULER* and forwards information to the queue. It can only push one data packet per cycle to the queue. Both in offline and online mode, however, it can receive a deadline and an event at the same time. For this reason, this component is clocked twice as fast as *hclk*. This enables it to wait on events in even cycles and wait on deadlines in odd cycles. Yet, it needs to be slower than *sclk* such that the queue can still process both data packets in time. As a result, it grants precedence to events. This is desired to compensate for the delay introduced by the *EVENTDELAY* and preserve the correct order of events and deadlines.

Formally, in even cycles this component computes:

$$\begin{aligned}
push^t &= valid\_ev^t \\
data^t &= ev^t \circ \bigvee_{i=1}^{n^l} (\text{dep}(i) \wedge ev^t [\sum_{j=1}^i (s_j + 1) - 1])
\end{aligned}$$

Here, *dep* is another static array of  $n^l$  bit wide registers where each bit represents a dependency between streams. I.e., if *dep*(*i*)[*j*] is on, output stream *j* transitively depends on input stream *i* and thus has to be evaluated with the current event. The respective dependencies are conjoined with  $ev[\sum_{j=1}^i (s_j + 1) - 1]$ , i.e., the bit indicating whether the current event carries a new value for input stream *i*. Overall, the data sent to the queue thus contains the event data, the time stamp of the event, and one bit per stream indicating whether the stream will be evaluated.

In odd cycles, the *data* signal only contains the streams affected by the deadline:

$$\begin{aligned}
push^t &= valid\_dl^t \\
data^t &= 0^{\sum(s_i+1)} \circ dl^t [\dots s_{ts}] \circ dl\_target(dl^t [s_{ts} \dots])
\end{aligned}$$

### 3.3 Input Buffering

The stalling mechanism in the *EVENTDELAY* and *SCHEDULER* is only necessary in offline mode. Two consecutive events  $e_i$  and  $e_{i+1}$  can have time stamps that skip several deadlines. In this case, the *SCHEDULER* repeatedly considers  $e_{i+1}$  as a new value and triggers the computation of a deadline until no more deadline is due. During this time, it raises the *hold* flag, so that the *EVENTDELAY* stalls  $e_{i+1}$  before sending it to the *HLQINTERFACE*. While stalling, the *EXTINTERFACE* can continue receiving events that are either lost, or override  $e_{i+1}$ . To prevent this, we add an input buffer of size  $\mathcal{L}$  in front of the *SCHEDULER* and *EVENTDELAY*. The required buffer size can be computed based on the input data. Assume that the HLC receives a new input value every  $\delta$  *hclk* cycles. The *backlog*  $bl(e_i)$  describes how many cycles it takes to fully process all entries currently in the buffer when receiving event  $e_i$ , including all deadlines induced by  $e_i$ .

$$\begin{aligned}
bl(e_1) &= 0 \\
bl(e_{i+1}) &= bl(e_i) - \min\{bl(e_i), \delta - 1\} + dld(e_{i+1})
\end{aligned}$$

Here,  $dld(e_i)$  is the number of periodic deadlines that become due when receiving  $e_i$ . Intuitively, between event  $e_i$  and  $e_{i+1}$ ,  $\delta - 1$  cycles pass without a new event, so we either process  $\delta - 1$  deadlines or events, or all entries in the buffer. Upon receiving  $e_{i+1}$ , we need to process an additional  $dld(e_i)$  deadlines plus the new event. At the same time, another cycle passes, so we can immediately process one event or deadline. This effectively eliminates the incoming event, so only  $dld(e_i)$  needs to be taken into account.

Let  $\mathcal{B}$  be a buffer of size  $\mathcal{L}$  with the following semantics, where  $\mathcal{B}_i^\eta$  is the *i*th entry of  $\mathcal{B}$  at cycle  $\eta$ :

$$\begin{aligned}
\mathcal{B}^0 &= \{\perp\}^{\mathcal{L}} \\
\mathcal{B}^{\eta+1} &= \begin{cases} \mathcal{B}^\eta \ll 1 & \text{if } \neg hold^{\eta+1} \wedge \neg valid\_its^{\eta+1} \\ \mathcal{B}^\eta & \text{if } hold^{\eta+1} \wedge \neg valid\_its^{\eta+1} \\ \mathcal{B}^\eta \oplus its^{\eta+1} & \text{if } hold^{\eta+1} \wedge valid\_its^{\eta+1} \\ (\mathcal{B}^\eta \ll 1) \oplus its^{\eta+1} & \text{if } \neg hold^{\eta+1} \wedge valid\_its^{\eta+1} \end{cases}
\end{aligned}$$

Here,  $\mathcal{B} \ll 1$  shifts the entire buffer content to the left, i.e., the first and thus oldest entry gets evicted, the  $n + 1$ st entry becomes the  $n$ th, and the last entry becomes  $\perp$ .  $\mathcal{B} \oplus v$  denotes that the first free entry of  $\mathcal{B}$ , i.e., the first  $k$  with  $\mathcal{B}_k = \perp$ , is replaced by  $v$ . If no such entry exists, the buffer overflows. Formally, the theorem states the following:

**THEOREM 3.1.** *If the buffer size  $\mathcal{L}$  maximizes  $bl$ , the buffer will never overflow:*

$$\mathcal{L} \geq \max\{bl\} \implies \forall \eta: \neg \text{valid\_its}^\eta \vee \neg \text{hold}^\eta \vee \mathcal{B}_\mathcal{L}^\eta = \perp$$

**PROOF.** We define an abstract buffer  $\tilde{\mathcal{B}}$  where each abstract entry corresponds to a concrete one in  $\mathcal{B}$ . Its value states how many clock cycles are required to process the deadlines induced by the respective concrete entry if it were the first one.

$$\tilde{\mathcal{B}}^0 = \{\perp\}^\mathcal{L}$$

$$\tilde{\mathcal{B}}^{\eta+1} = \begin{cases} \text{dec}(\tilde{\mathcal{B}}^\eta) & \text{if } \tilde{\mathcal{B}}_1^\eta > 0 \wedge \neg \text{valid\_its}^{\eta+1} \\ \text{dec}(\tilde{\mathcal{B}}^\eta) \oplus \text{dld}(\text{its}^{\eta+1}) & \text{if } \tilde{\mathcal{B}}_1^\eta > 0 \wedge \text{valid\_its}^{\eta+1} \\ \tilde{\mathcal{B}}^\eta \ll 1 & \text{if } \tilde{\mathcal{B}}_1^\eta = 0 \wedge \neg \text{valid\_its}^{\eta+1} \\ (\tilde{\mathcal{B}} \ll 1) \oplus \text{dld}(\text{its}^{\eta+1}) & \text{if } \tilde{\mathcal{B}}_1^\eta = 0 \wedge \text{valid\_its}^{\eta+1} \end{cases}$$

Here,  $\text{dec}(\tilde{\mathcal{B}})$  reduces the value of the first and thus oldest value by one, which represents that a deadline induced by the event was processed. We define the size of an entry in  $\tilde{\mathcal{B}}$  as

$$\text{size}(\tilde{\mathcal{B}}_i^\eta) = \begin{cases} 0 & \text{if } \tilde{\mathcal{B}}_i^\eta = \perp \\ \tilde{\mathcal{B}}_i^\eta + 1 & \text{otherwise} \end{cases}$$

The proof follows from three facts.

1)  $bl$  is the sum of the size of  $\tilde{\mathcal{B}}$ 's entries, i.e., for any event  $e_i$  that reaches the buffer in cycle  $\eta_i$ , the following holds:

$$bl(e_i) = \sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_i}) \quad (1)$$

Proof by induction on the event sequence consisting of the events  $e_1, e_2, \dots$ . Assume  $\eta_i$  is the clock cycle in which  $e_i$  arrives at the buffer. For  $\eta_0$ :

$$\sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}_0^{\eta_0}) = \sum_{j=1}^{\mathcal{L}} 0 = 0 = bl(e_0)$$

In the induction step, we go from  $\eta_i$  to  $\eta_{i+1}$ . Note that these two points in time are separated by  $\delta$  clock cycles, i.e.,  $\eta_{i+1} = \eta_i + \delta$ . In each of these steps, no new value arrives at the buffer, so  $\forall j \in \{1, \dots, \delta - 1\}: \neg \text{valid\_its}^{\eta_i+j}$ . Thus, by definition of  $\tilde{\mathcal{B}}$ , the sum of the abstract entries always decreases by 1 for each  $hclk$  cycle unless the buffer is already empty. In this case, the values does not change. In cycle  $\eta_{i+1}$ , however, the buffer additionally receives a new value,

so the sum of the entries also increases by  $\text{dld}(e_{i+1}) + 1$ . Formally:

$$\begin{aligned} & \sum_{j=0}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_{i+1}}) \\ &= \sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_{i+1}-1}) + (\text{dld}(e_{i+1}) + 1) - 1 \\ &= \sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_i}) - \min\left\{\sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}_j^{\eta_i}), \delta - 1\right\} + \text{dld}(e_{i+1}) \\ &= bl(e_i) - \min\{bl(e_i), \delta - 1\} + \text{dld}(e_{i+1}) \quad (\text{IH}) \\ &= bl(e_{i+1}) \end{aligned}$$

The next fact can be proven using Equation (1):

2) *The abstract buffer cannot overflow*, more concretely:

$$\mathcal{L} \geq \max\{bl\} \implies \forall \eta: \neg \text{valid\_its}^\eta \vee \tilde{\mathcal{B}}_1^{\eta-1} = 0 \vee \tilde{\mathcal{B}}_\mathcal{L}^{\eta-1} = \perp \quad (2)$$

Assume  $\mathcal{L} \geq \max\{bl\}$  and  $\text{valid\_its}^\eta \wedge \tilde{\mathcal{B}}_1^{\eta-1} > 0 \wedge \tilde{\mathcal{B}}_\mathcal{L}^{\eta-1} \neq \perp$ . Since  $\text{valid\_its}^\eta$ , we know that a new event arrived. If it is the first event, i.e.,  $\eta = \eta_0$ , the contradiction follows from the definition of  $\tilde{\mathcal{B}}$ . Otherwise, let  $\eta = \eta_{i+1}$ . We inspect the last  $\delta$  steps. We know that no new value arrived, and because  $\tilde{\mathcal{B}}_\mathcal{L}^{\eta-1} \neq \perp$  holds, there was no shift.

$$\tilde{\mathcal{B}}_1^{\eta_{i+1}-1-\delta} = \tilde{\mathcal{B}}_1^{\eta_i-1} = \delta + \tilde{\mathcal{B}}_1^{\eta_{i+1}-1} \geq \delta + 1 \quad (3)$$

As a result:

$$bl(e_i) = \sum_{j=1}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_i}) \quad (\text{Eq. (1)})$$

$$\geq \sum_{j=2}^{\mathcal{L}} \text{size}(\tilde{\mathcal{B}}^{\eta_i}) + \delta + 1 \quad (\text{Eq. (3)})$$

$$\geq \delta + 1 + \mathcal{L} - 1 \quad (\delta > 0)$$

$$\geq \mathcal{L} + 1$$

This contradicts  $\mathcal{L} \geq \max\{bl\}$ .

3) *Each entry of the abstract buffer corresponds to an entry in the concrete buffer.*

$$\forall \eta, i: \tilde{\mathcal{B}}_i^\eta = \perp \iff \mathcal{B}_i^\eta = \perp \quad (4)$$

The equation holds by the definitions of  $\tilde{\mathcal{B}}$  and  $\mathcal{B}$ . The proof itself consists of correct bookkeeping of the buffer states and respective signal values.

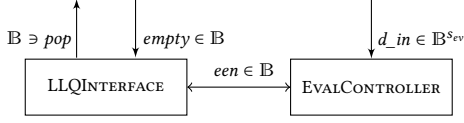
By Equation (4) we know that each empty entry in the abstract buffer is also empty in the concrete buffer. Moreover, Equation (2) verifies that the abstract buffer never overflows. Thus, the concrete buffer cannot overflow as well, concluding the proof.  $\square$

### 3.4 Low-level Controller (LLC)

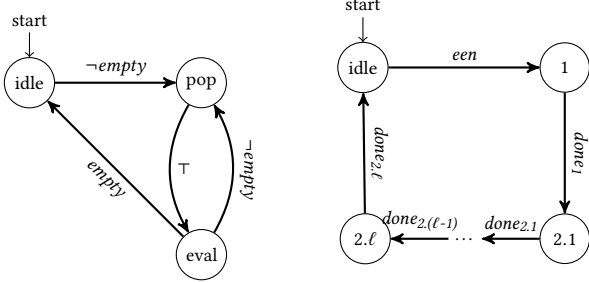
The LLC receives elements from the queue and evaluates streams according to the information received. After the evaluation, it checks for violated properties and triggers an alarm if appropriate.

As can be seen in Figure 5, it consists of a LLQINTERFACE component which communicates with the queue and triggers an evaluation process taking place in the EVALCONTROLLER.





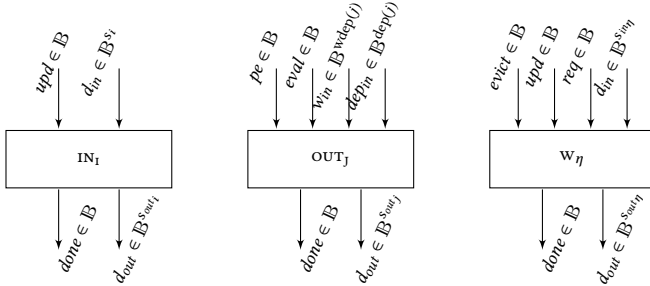
**Figure 5: Schematic of the Low-level Controller receiving event and deadline information from the queue and evaluating streams accordingly.**



(a) The LLQINTERFACE handles the communication with the queue in pop, and waits in eval until the evaluation finished.

(b) The EVALCONTROLLER manages the evaluation. State 1 treats input streams, 2.1 through 2.l output streams according to the evaluation order.

**Figure 6: State machines for the LLQINTERFACE and the EVALCONTROLLER**



**Figure 7: Input and output signals of input and output streams.**

*LLQInterface.* This component consists of a three-state machine depicted in Figure 6a. In the *idle* state, it waits on new inputs from the queue. On a falling edge of *empty*, it transitions into the *pop* state, rising the *pop* signal for one *selk* cycle. At the end of this cycle, it unconditionally transitions to *eval*, setting the *evaluation enable een* latch. This signals the EVALCONTROLLER that valid data is on the *d\_in* wire, so an evaluation can be started. After the evaluation is completed, EVALCONTROLLER clears the *een* signal. Depending on the current queue state, it transitions back to *idle* or *pop*.

*EvalController.* This component is a state machine as depicted in Figure 6b with  $\ell + 2$  states where  $\ell = \max(\ell \in \mathbb{N} \mid \exists s_1 \dots s_\ell : s_1 < \dots < s_\ell)$  is the number of layers of the evaluation order (see Figure 6b). In addition to the state machine, there are  $n^\downarrow / n^\uparrow / n^w$  input/output/window components. In the following, components and

signals indexed with  $i, j, \eta$  refer to inputs, outputs, and windows, respectively.

In the *idle* state, the EVALCONTROLLER waits on a rising edge of *een*, on which it transitions to state 1. This state corresponds to a so-called *pseudo-extension* phase, where all output streams that get a new value in this evaluation cycle are extended by a pseudo value  $\#$ . This value will never be used in a computation but allows for resolving offsets correctly without shifting the offsets depending on the evaluation status of the target stream. Input streams are immediately extended by their new values, and windows evict outdated buckets. Thus:

$$\begin{aligned} \forall i \leq n^\downarrow : upd_i &= d_{in}[\sum_{n \leq i} (s_n + 1)] \\ \forall j \leq n^\uparrow : upd_j &= d_{in}[\sum (s_i + 1) + s_{ts} + j] \\ \forall \eta \leq n^w : evict_\eta &= 1 \end{aligned}$$

The structure of input, output and window components is depicted in Figure 7. In the input stream components we get the following behavior for a rising edge in *upd<sub>i</sub>* where  $\kappa(i)$  describes the greatest offset of any lookup with target  $i$ :

$$\begin{aligned} done^t &= upd^t \\ \mathbf{R}_n^0 &= 0^{s_i+1} \\ \mathbf{R}_n^{t+1} &= \begin{cases} \mathbf{R}_{n+1}^t & \text{if } upd^{t+1} \wedge n \neq \kappa(s_i) \\ \mathbf{R}_n^t & \text{if } \neg upd^{t+1} \\ d_{in}^{t+1} \circ 1 & \text{if } upd^{t+1} \wedge n = \kappa(s_i) \end{cases} \\ d_{out}^0 &= 0^{\kappa(i) \cdot (s_i+1)} \\ d_{out}^{t+1} &= \mathbf{R}_1^t \circ \dots \circ \mathbf{R}_{\kappa(s_i)}^t \end{aligned}$$

By storing  $\kappa(i)$  values for any stream  $i$ , all offsets can be resolved when evaluating stream expressions.

Output streams on a rising edge of *pe* behave as follows:

$$\begin{aligned} done^t &= pe^t \\ \mathbf{R}_n^0 &= 0^{\kappa(j) \cdot (s_j+1)} \\ \mathbf{R}_n^{t+1} &= \begin{cases} \# & \text{if } n = \kappa(j) \\ \mathbf{R}_{n+1}^t & \text{otherwise} \end{cases} \\ d_{out}^0 &= 0^{\kappa(j) \cdot (s_j+1)} \\ d_{out}^{t+1} &= \mathbf{R}_1^t \circ \dots \circ \mathbf{R}_{\kappa(s_j)}^t \end{aligned}$$

For windows, the number of buckets is  $\beta$ , i.e., the length of the window  $dur_\eta$  multiplied with the extend frequency  $f_\eta$  of stream in which the window occurs. On a rising edge of *evict*, *d\_in* carries the current time stamp in the first  $s_{ts}$  bits. The window requires this information to decide whether new buckets are outdated. If so, the values of all registers are shifted and the now-empty bucket is initialized with  $\varepsilon$ . The internal **T** register stores the time when the

next bucket becomes outdated.

$$\begin{aligned} \mathbf{T}^0 &= 0^{s_{ts}} \\ \mathbf{T}^{t+1} &= \begin{cases} \mathbf{T}^t & \text{if } d_{in}[\dots s_{ts}] \leq \mathbf{T}^t \\ \mathbf{T}^t + f_\eta & \text{otherwise} \end{cases} \\ done^0 &= 0 \\ done^{t+1} &= d_{in}[\dots s_{ts}] \leq \mathbf{T}^t \\ \mathbf{R}_n^0 &= \varepsilon \\ \mathbf{R}_n^{t+1} &= \begin{cases} \varepsilon & \text{if } n = \beta \wedge d_{in}[\dots s_{ts}] > \mathbf{T}^t \\ \mathbf{R}_{n+1}^t & \text{if } n \neq \beta \wedge d_{in}[\dots s_{ts}] > \mathbf{T}^t \\ \mathbf{R}_n^t & \text{if } d_{in}[\dots s_{ts}] \leq \mathbf{T}^t \end{cases} \end{aligned}$$

Signal  $done_j$  indicates that phase 1 of the evaluation is complete:

$$done_1 = \bigwedge_{i \leq n^l} upd_i \implies done_i \wedge \bigwedge_{j \leq n^l} pe_j \implies done_j \wedge \bigwedge_{\eta \leq n^*} done_\eta$$

Note that the implication ensures that a  $done$  signal is only relevant, if the respective component was enabled.

After  $done_j$  is raised, the EVALCONTROLLER transitions to phase 2 via state 2. 1. In the 2. x states, streams are successively extended according to the evaluation order and windows are updated whenever the target stream computed a new value. Wires connect streams and windows w.r.t. their dependencies, i.e., all streams output a sequence of values coupled with a bit indicating its validity. Invalid values are then replaced with the default values specified in the stream expression. Window lookups require an additional computation step, initiated by the  $req$  signal.

Formally, when transitioning to state 2. x with  $1 \leq x \leq \ell$ , the EVALCONTROLLER raises the update signals for outputs and windows if appropriate, i.e., if the stream is in the respective evaluation layer and the HLC indicated that the stream is affected.

$$\begin{aligned} eval_j &= j \in \text{layer}(x) \wedge d_{in}[\sum (s_i + 1) + s_{ts} + j] \\ upd_\eta &= d_{out_{tar(\eta)}}[s_{tar(\eta)}] \end{aligned}$$

On a rising edge of  $eval_j$ , the output stream computes its new value and updates its internal state:

$$\begin{aligned} done^t &= eval^t \\ \mathbf{R}_n^{t+1} &= \begin{cases} \text{evalexpr}(j) \circ 1 & \text{if } eval^{t+1} \wedge n = \kappa(j) \\ \mathbf{R}_n^t & \text{otherwise} \end{cases} \\ d_{out}^{t+1} &= \mathbf{R}_1^t \circ \dots \circ \mathbf{R}_{\kappa(s_j)}^t \end{aligned}$$

Here,  $\text{evalexpr}(j)$  is the result of evaluating the stream expression of stream  $j$ . The computation can be split into several computation steps depending of the size of the expression to increase the maximum system clock frequency. In this case, the  $done$  bit cannot be set immediately after receiving the  $eval$  command. Note that only # values are overwritten in this step and the valid bit is set. In sliding windows, a new values is added by applying the  $map$  function and reducing it onto the last bucket.

$$\begin{aligned} \mathbf{R}_\beta^{t+1} &= \mathbf{R}_\beta^t \oplus \text{map}(d_{in}^{t+1}) \\ done^t &= upd^t \end{aligned}$$

It requires an additional step to compute the new value of the sliding window. This process is initiated by the EVALCONTROLLER by raising the  $req_\eta$  flag after the window's target stream was computed.

All bucket values get reduced using the aggregation's reduction function  $\oplus$ , and finalized afterwards. Since  $\oplus$  is associative and the number of buckets is a compile time constant, the reduction is structured as a binary tree with logarithmic depth in the number of buckets. This triggers the following behavior in the window:

$$\begin{aligned} d_{out}^{t+1} &= \text{fin}(\mathbf{R}_1^t \oplus \dots \oplus \mathbf{R}_\beta^t) \\ done_{2.x}^t &= req^t \end{aligned}$$

## 4 CASE STUDY

We validated the compilation with three case studies. The first two monitor a network and an avionic and describe realistic scenarios, whereas the third one consists of synthetic data and emphasizes the benefits of the parallel evaluation structure presented in Section 3. All specifications were compiled into VHDL code and then synthesized on a Zynq-Z-7010 ARM/FPGA SoC Trainer Board<sup>3</sup>, which is logic-equivalent to an Artix-7 FPGA. The Zynq-7000 features 4.400 logic slices, each with four 6-bit input LUTs and 8 flip flops.

Note that the specifications in the benchmarks are simplified for illustration purposes. The current prototype does not support a floating or fixed point unit. The limitation is a result of technical incompatibilities in the Xilinx synthesizing software; from a theoretical standpoint, the inclusion of a floating-point unit is possible. This results however in a larger circuit realization of the specifications.

### 4.1 Avionics

Figure 8 shows a specification for a drone. Input events consist of longitude and latitude values, the velocity and the number of GPS satellites in range. The GPS module is supposed to send values for the longitude and latitude with frequency 10 Hz. Output stream  $\text{gps\_freq}$  counts the number of samples received within a second and checks if it falls below 9. In this case, the first trigger reports the unexpectedly low sample frequency. The second trigger reports a warning when the drone's velocity drops below 700, requiring that the velocity was greater than 700 before that. For the third trigger, we use a simplified reconstruction of the distance the drone traveled using the Pythagorean theorem. A more realistic approximation can be obtained e.g. by using the haversine function. The square root computation is realized using the constant-time function proposed by Li and Chu [29]. The distance is then discretely differentiated to compute the velocity according to the GPS module. This allows for cross-validating sensor values by comparing the sensed input velocity with the computed one. If the two values deviate too strongly, an alarm is raised. Lastly, we detect hover phases by integrating either velocity value and checking whether it lays below a threshold value.

We compiled the specification to VHDL and synthesized a circuit on the Zynq-7000 board. We report the resource consumption in terms of required flip-flops (FF), look-up tables (LUT), multiplexers (MUX), adders (CA), and multipliers (MULT) for each component below, where "Mon" describes the entire synthesized monitor:

<sup>3</sup>[https://reference.digilentinc.com/reference/programmable-logic/zybo/reference-manual?\\_ga=2.102758273.1814454663.1555084001-1980681841.1546416239](https://reference.digilentinc.com/reference/programmable-logic/zybo/reference-manual?_ga=2.102758273.1814454663.1555084001-1980681841.1546416239)

Component	FF	LUT	MUX	CA	MULT
Mon	3036	3685	26	656	18
HLC	901	156	0	22	0
Q	543	442	0	43	0
LLC	1281	2820	0	576	18

Note that the amount of resources like flip-flops of the entire monitor is not equal to the sum of the resources of all components. The difference is required for internal tasks such as signal management. One can see that most flip-flops reside in the LLC because it manages the persisted values of all streams. The HLC requires around 70% as many, which can be contributed to the fact that each component of the HLC contains internal registers while the greatest offset in the specification is only  $-1$ , reducing the memory requirement of the LLC. The overwhelming majority of look-up tables, adders, and multipliers reside in the LLC which was expected given that this component implements the evaluation logic. The 18 multipliers are required for squaring the  $\delta$ -values and computing the integral window.

The power consumption amounted to 0.121 W when idle and 1.620 W when processing.

We tested the monitor in online mode with sensor data created in a simulation using the ArduPilot<sup>4</sup> Copter<sup>5</sup> drone simulator. The simulator consisted of a multicopter flying over the campus of a university. Sensor information was piped to the monitor over a serial port. Evaluating events and periodic deadlines took on average 428 system clock cycles with a period  $\xi = 100$  MHz. Thus, each event took on average 4.28  $\mu$ s to be processed. Here, the worst slack amounted to 1.653 ns.

## 4.2 Network Monitoring

The network monitoring exerted an immense pressure on the monitor due to the sheer amount of input data received in a short amount of time. In this setting it is also reasonable to forgo any assumption on the input frequency.

The specification in Figure 9 fixes the IP of one particular server and checks network traffic based on the source and destination IP of requests, TCP flags, and the length of the payload. First, the length stream is filtered based on whether the server is the target and the request pushes data. We sum up the filtered stream for a second and trigger an alert if the amount of data spikes over 10 MB. Moreover, we count the number of opened and closed incoming connections and issue an alert if the server attempts to close more connections that were opened. Lastly, we check for a significant amount of incoming connections in a short amount of time.

Due to the lower complexity of the specification, the resource consumption is also generally lower compared to the avionics example. The number of look-up tables decreases by around 60%, adders by 65% and multipliers by 100%. The number of flip-flops only decreases by around 38% since there is no significant difference in the number of sliding windows and lookup expressions in the two specifications, but integral windows require 5-times as much memory as summation and count windows.

Component	FF	LUT	MUX	CA	MULT
Mon	1905	1533	23	226	0
HLC	550	161	0	37	0
Q	330	342	0	28	0
LLC	895	927	0	161	0

The power consumption amounted to 0.120 W when idle and 1.570 W when processing, so there is no significant difference between the two specifications.

We tested the implementation with data from the Mid-Atlantic Collegiate Cyber Defense Competition (MACCDC)<sup>6</sup>. We re-played the log data in real time using the time stamps provided.

While the evaluation process is simpler, the HLC remains mostly the same. Thus, the amount of system clock cycles required per event only decreases by around 25%, the response time for a single event is 3.2  $\mu$ s on average. The worst slack time, however, increased by 150% to 4.0 ns. This allows for safely increasing the system clock frequency by up to 200 MHz. The reason for this is that the square root computation in the avionics specification has a significantly greater depth than all operation performed while monitoring the network. Since the computation is taken out in a single cycle, the slack time decreases significantly.

## 4.3 Parallelization

Section 3.4 presents a compilation that produces a highly parallel evaluation process by identifying modular structures within the specification. The modularity is maximized when a specification contains a large number of independent streams. Practical examples of this kind of specification are command-response or geofencing specifications. Here, each reaction and each face of the fence constitutes an independent stream, allowing for a parallel evaluation.

More concretely, consider a system that receives different commands from an external entity and needs to verify the system health depending on the kind of command. Such a specification can be found in Figure 10. The highly disjunctive nature allows for perfect parallelization: each output stream solely depends on input streams. In this case study, the specification is realized twice, once as proposed in Section 3, and once without the parallelization of the evaluation. Purposefully declared spurious dependencies between successive output streams enforce a sequential evaluation. Figure 10 contains an extract of the specification.

Neither the size of the realization, nor the power consumption when idle varied between the realizations. A stress-test successively increases the input data rate until the LLC can no longer process events in time. For this, the companion processor on the Zynq sends events to the FPGA and measures the time it takes for the FPGA to produce an output. This measurement produces more robust result than the communication over a bus in the preceding case studies but can only be applied in the absence of periodic streams. When processing events in the maximum frequency for each realization, the parallel realization requires slightly more power (1.582 W) than the sequential one (1.581 W). As opposed to that, the execution time varies significantly. The sequential execution requires 43.83  $\mu$ s, whereas the speed of the parallel execution exceeds the computation speed of the processor, which is up to 866 MHz, i.e. 3.77  $\mu$ s between

<sup>4</sup><http://ardupilot.org/>

<sup>5</sup><http://ardupilot.org/copter/index.html>

<sup>6</sup><https://www.netresec.com/?page=MACCDC>

```

input lat, lon, velo: Int32
input gps: UInt8

output gps_freq@1Hz : bool :=
  lat.aggregate(over:1s,using:count).defaults(to:10) < 9
trigger gps_freq "GPS frequency less than 9 Hz"

output fast := velo > 700
trigger fast.offset(by:-1).defaults(to:false) & !fast
  "Slowing down"

output gps_dist := sqrt( $\delta(\text{lon})^2 + \delta(\text{lat})^2$ )
output gps_velo := gps_dist /  $\delta(\text{time})$ 
trigger abs(gps_velo - velo) > 10 "Sensor deviation"

output hovering@1Hz :=
  velo.aggregate(over:5s,using: $\int$ ).defaults(to:5) < 1
trigger hovering "Little distance covered"

```

Figure 8: RTLOLA specification for monitoring a drone.

```

constant server: Int32 = ...
input src, dst: Int32
input fin, push, syn: bool
input length: Int32

output receiver := dst = server
trigger @1Hz
  receiver.aggregate(over:0.5s,using: $\Sigma$ ) > 10000
  "Many incoming connections"

output received := if receiver & push
  then 0
  else length
output workload@1Hz :=
  received.aggregate(over:1s,using: $\Sigma$ )
trigger workload > 107 "Workload too high"

output opened :=
  open.offset(by:-1).defaults(to:0) +
  (if dest = server & syn then 1 else 0)
output closed :=
  closed.offset(by:-1).defaults(to:0) +
  (if dest = server & fin then 1 else 0)
trigger open - closed < 0
  "Closed more connection than were open"

```

Figure 9: RTLOLA specification for monitoring network traffic.

sending an event and attempting to read the output. As a result, the measured 3.77  $\mu\text{s}$  constitute an upper bound on the actual response time. Practically, this means that if the processor sends events to the FPGA with its maximum frequency, the parallel realization can process all events, whereas the sequential one loses 89% of the data.

## 5 CONCLUSION

We have presented a hardware-based monitoring approach for stream-based real-time specifications by compiling RTLOLA specifications to circuits on FPGAs. The resulting circuits are small and efficient. Unlike interpreter-based approaches, the compiler limits

```

input cmd: Int16
input height, x, y, ...: Int32

output health_crit_1: Bool := height < 400
trigger health_crit_1 & cmd = 1
...

output health_crit_512: Bool :=
  x > 700  $\vee$  y < 250  $\wedge$  height > 300
trigger health_crit_512 & cmd = 512

```

Figure 10: RTLOLA specification for a highly parallelizable property.

the circuits to the operations in the specification and allows for a high degree of parallelization. The presented case studies show that FPGA-based stream-monitoring is feasible for non-trivial specifications. While we used a small board, the available resources were only utilized by less than 50% and the power consumption was around 1.5 W under maximal pressure. This makes the approach suitable for integration into embedded systems without draining the available resources.

Building on the work presented in this paper, the next step is to extend the FPGA approach to stream specifications with parameterization [16] and to investigate the applicability of FPGA-based monitoring in distributed architectures.

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