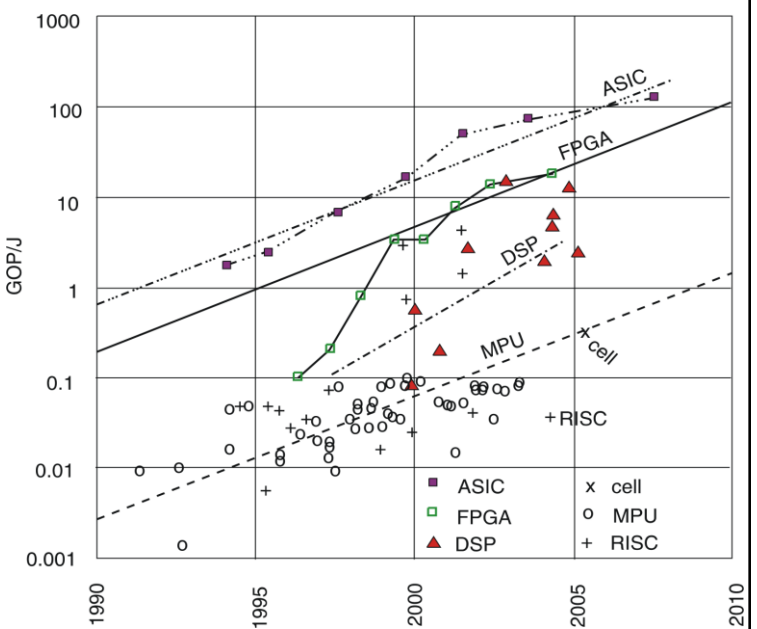
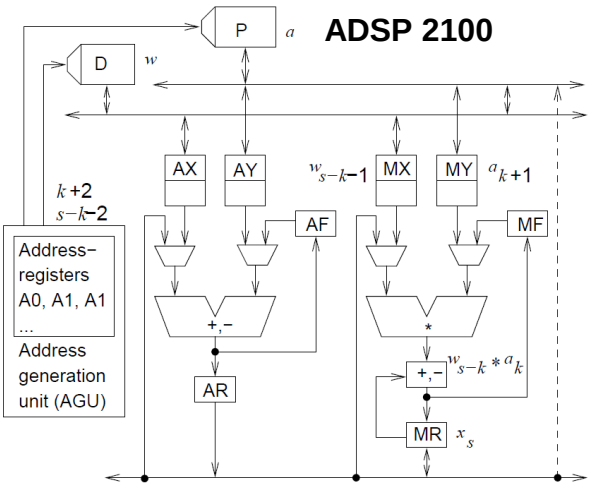
Embedded Systems 13

REVIEW: Energy



REVIEW: DSP



$$x_s = \sum_{k=0}^{n-1} w_{s-k} * a_k$$

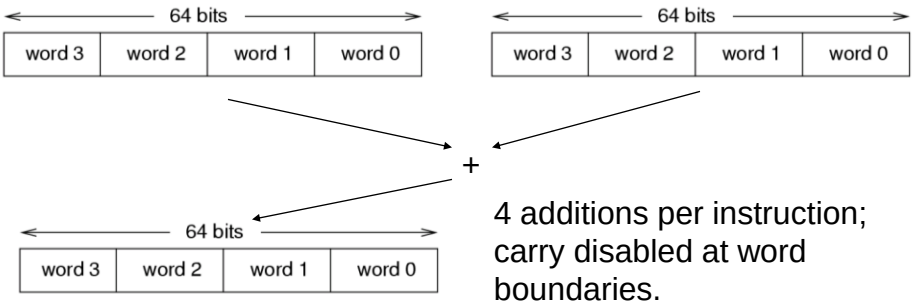
outer loop over sampling times t_s

```
{ MR:=0; A1:=1; A2:=s-1;
  MX:=w[s]; MY:=a[0];
  for (k=0; k <= (n−1); k++)
   { MR:=MR + MX * MY;
     MX:=w[A2]; MY:=a[A1];
     A1++; A2−−;
    }
  x[s]:=MR;
}
```


REVIEW: Single-instruction, multiple-data (SIMD)

- Multimedia instructions exploit that many registers, adders etc are quite wide (32/64 bit),
- whereas most multimedia data types are narrow (e.g. 8 bit per color, 16 bit per audio sample per channel)

☞ 2-8 values can be stored per register and added. E.g.:



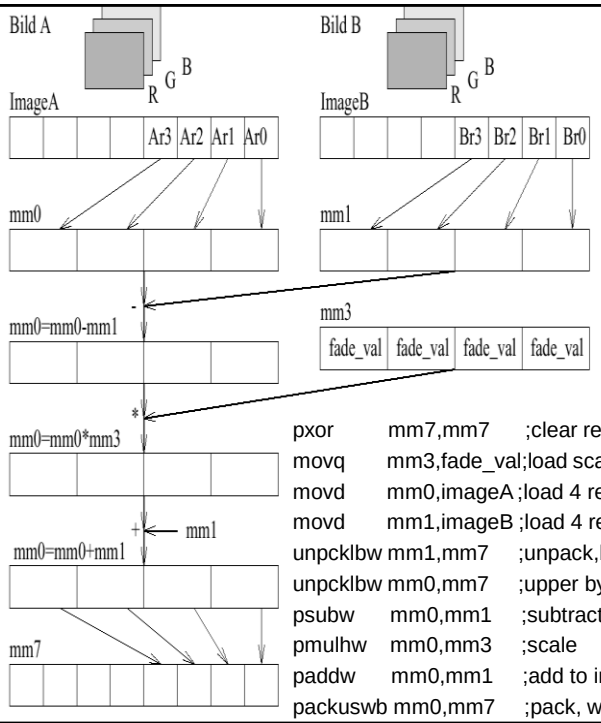
4 additions per instruction; carry disabled at word boundaries.

Pentium MMX

Example: Scaled interpolation between two images

Next word = next pixel, same color.

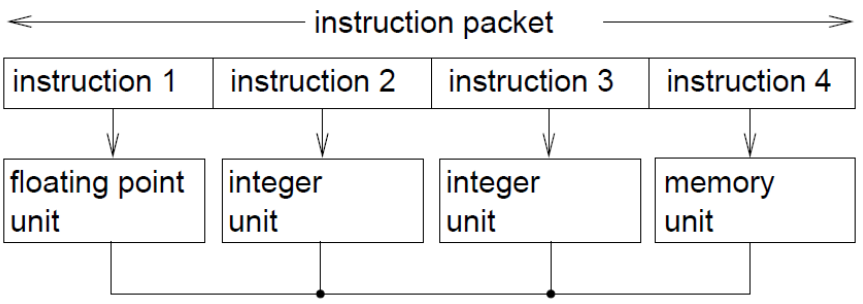
4 pixels processed at a time.




```
pxor       mm7,mm7      ;clear register mm7
movq       mm3,fade_val;load scaling value
movd       mm0,imageA ;load 4 red pixels for A
movd       mm1,imageB ;load 4 red pixels for B
unpcklbw mm1,mm7     ;unpack,bytes to words
unpcklbw mm0,mm7     ;upper bytes from mm7
psubw      mm0,mm1     ;subtract pixel values
pmulhw     mm0,mm3     ;scale
paddw      mm0,mm1     ;add to image B
packuswb mm0,mm7     ;pack, words to bytes
```

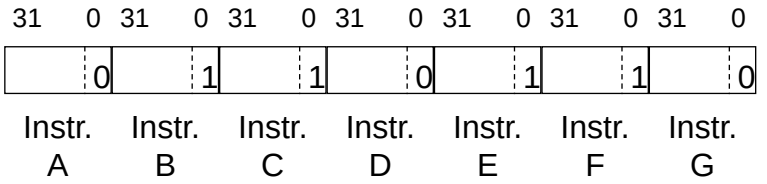

REVIEW: VLIW

- Instructions included in long instruction packets. Instruction packets are assumed to be executed in parallel.
- Fixed association of packet bits with functional units.



EPIC: TMS 320C6xx as an example

1 Bit per instruction encodes end of parallel exec.



Cycle	Instruction		
1	A		
2	B	C	D
3	E	F	G

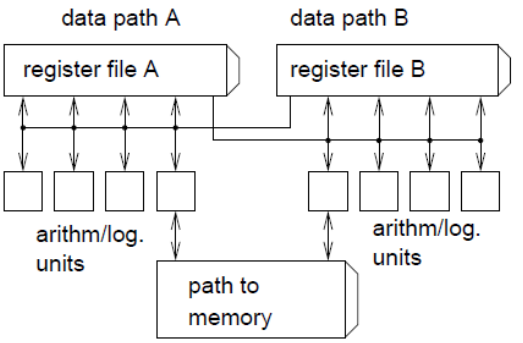
Instructions B, C and D use disjoint functional units, cross paths and other data path resources. The same is also true for E, F and G.

Parallel execution cannot span several packets.

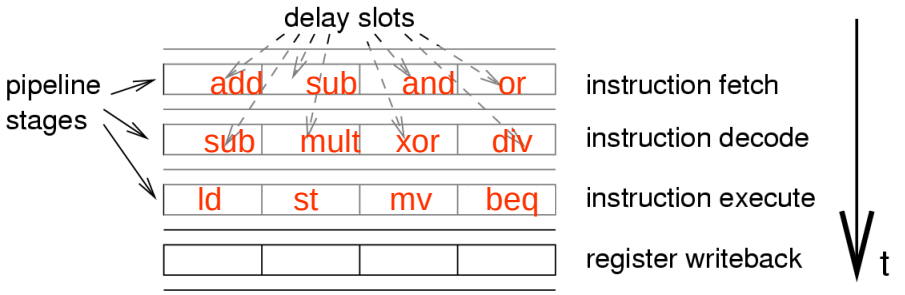
Partitioned register files

- Many memory ports are required to supply enough operands per cycle.
- Memories with many ports are expensive.

☞ Registers are partitioned into (typically 2) sets, e.g. for TI C60x:



REVIEW: Branch delay penalty



The execution of many instructions has been started before it is realized that a branch was required.
Nullifying those instructions would waste compute power

- ☞ Executing those instructions is declared a feature, not a bug.
- ☞ How to fill all “delay slots“ with useful instructions?
- ☞ Avoid branches wherever possible.

Predicated execution: Implementing IF-statements „branch-free“

Conditional Instruction „[c] I“ consists of:

- **condition c**
- **instruction I**

c = true => I executed
c = false => NOP

Predicated execution: Implementing IF-statements „branch-free“: TI C6x

```
if (c)
{ a = x + y;
  b = x + z;
}
else
{ a = x - y;
  b = x - z;
}
```

Conditional branch

```
      [c] B L1
          NOP 5
          B L2
          NOP 4
          SUB x,y,a
      ||  SUB x,z,b
L1:       ADD x,y,a
      ||  ADD x,z,b
L2:
```

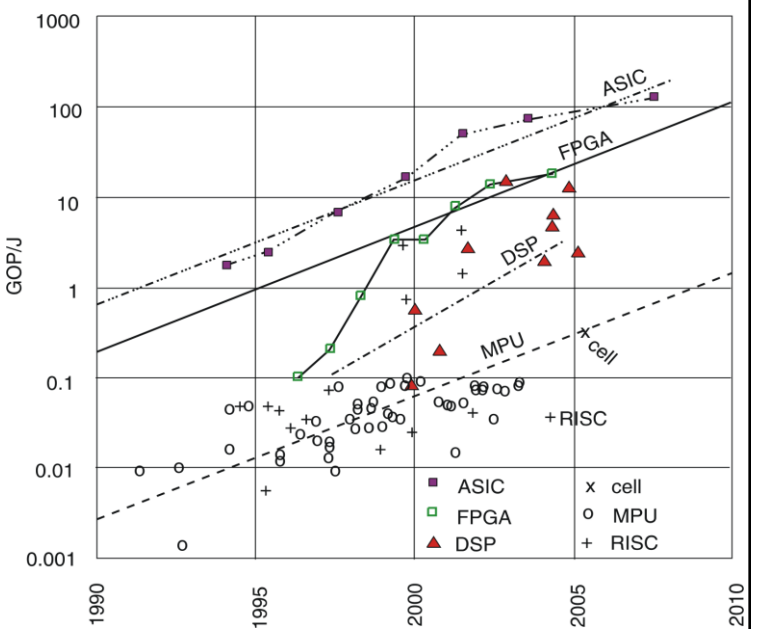
max. 12 cycles

Predicated execution

```
     [c]  ADD x,y,a
|| [c]  ADD x,z,b
|| [!c] SUB  x,y,a
|| [!c] SUB  x,z,b
```

1 cycle

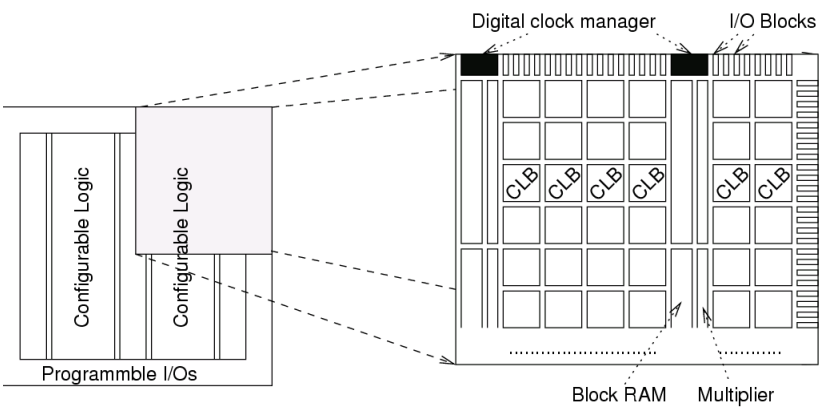
REVIEW: Energy



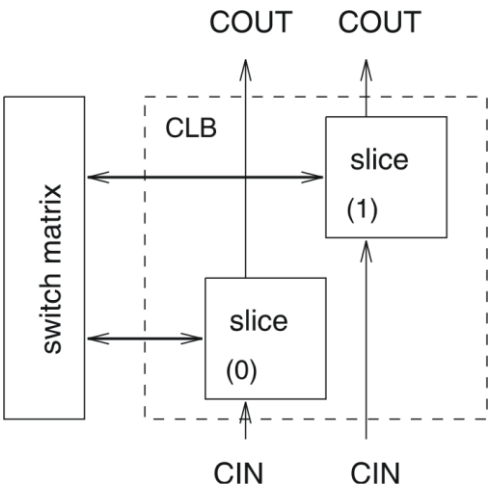
Reconfigurable Logic

- Full custom chips may be too expensive, software too slow.
- Combine the speed of HW with the flexibility of SW
  - ☞ HW with programmable functions and interconnect.
  - ☞ Use of configurable hardware;
    common form: field programmable gate arrays (FPGAs)
- ☞ Applications: bit-oriented algorithms like
  - encryption,
  - fast “object recognition“ (medical and military)
  - Adapting mobile phones to different standards.
- Popular devices from
  - XILINX (XILINX Virtex 6 are recent devices)
  - Actel, Altera and others

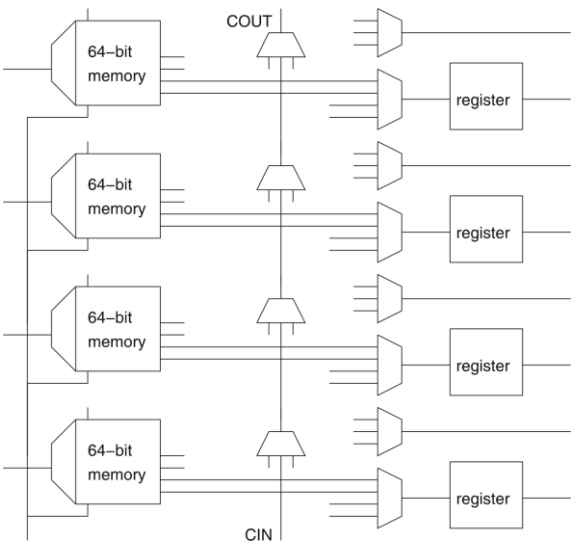
Floor-plan of VIRTEX II FPGAs



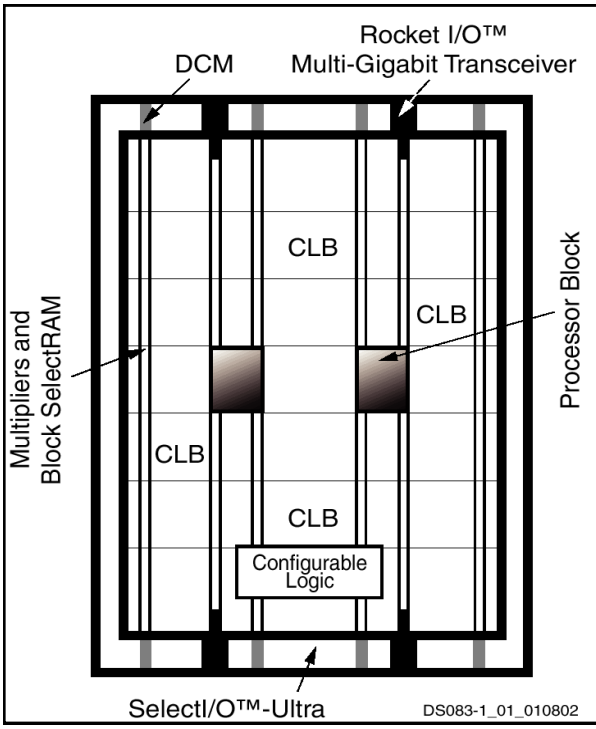
Virtex 5 Configurable Logic Block (CLB)



Virtex 5 Slice (simplified)



Memories typically used as look-up tables to implement any Boolean function of ≤ 6 variables.



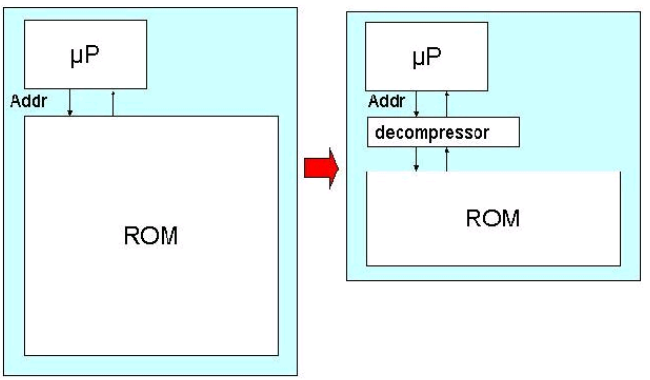
Virtex II Pro Devices include up to 4 PowerPC processor cores

Virtex 5 devices include up to 2 PowerPC processor cores

[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

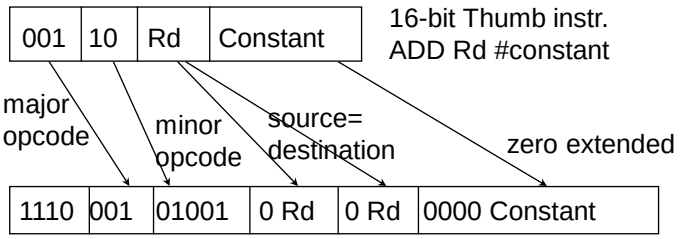
Code-size efficiency

- **CISC machines**: RISC machines designed for run-time-, not for code-size-efficiency
- **Compression techniques:** key idea



Code-size efficiency

- **Compression techniques (continued):**
  - 2nd instruction set, e.g. ARM Thumb instruction set:



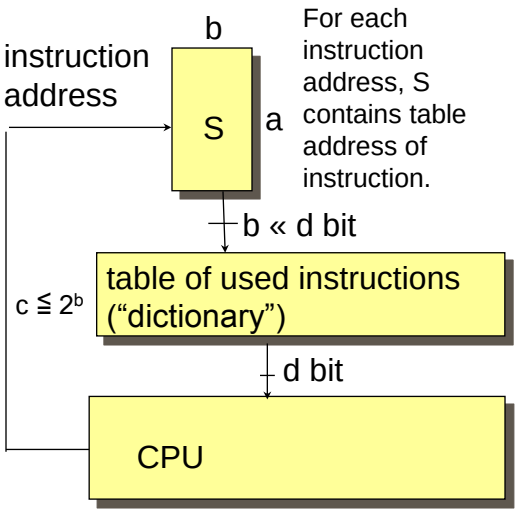
Dynamically decoded at run-time

- Reduction to 65-70 % of original code size
- 130% of ARM performance with 8/16 bit memory
- 85% of ARM performance with 32-bit memory

[ARM, R. Gupta]

Same approach for LSI TinyRisc, …
Requires support by compiler, assembler etc.

Dictionary approach



Uncompressed storage of *a d*-bit-wide instructions requires *axd* bits.

In compressed code, each instruction pattern is stored only once.

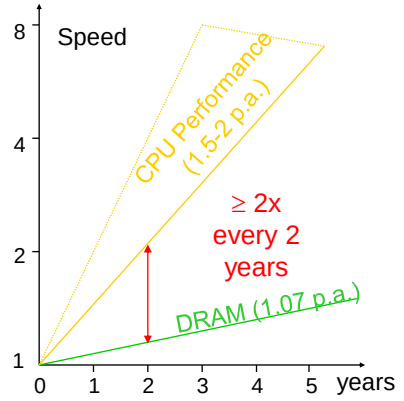
small

Hopefully, *axb+cxd < axd.*

Called nanoprogramming in the Motorola 68000.

Memory

- Speed gap between processor and main DRAM increases



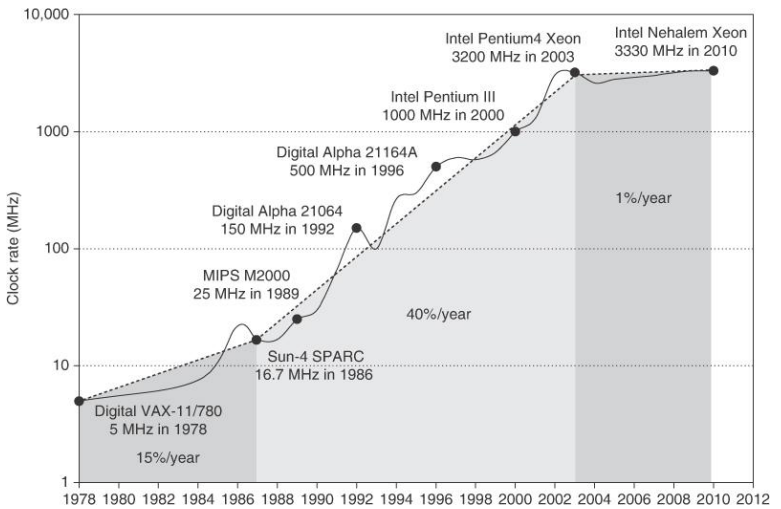
Similar problems also for embedded systems

☞ Memory access times >> processor cycle times

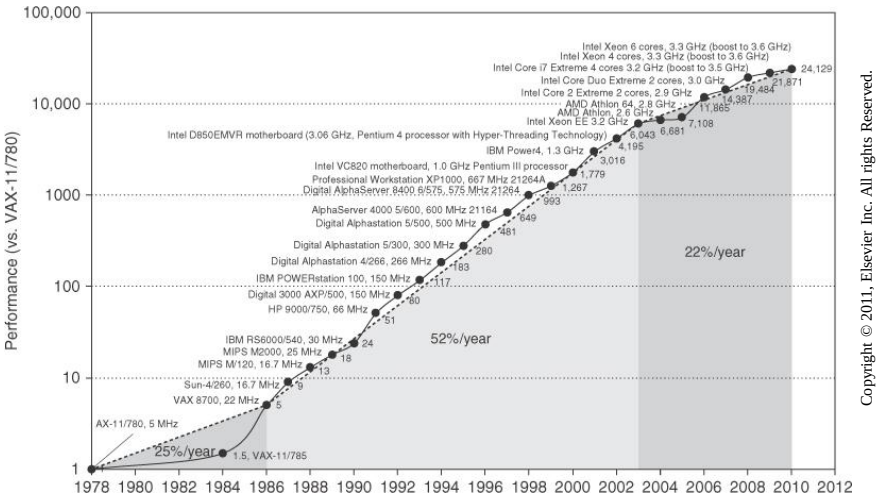
☞ "Memory wall" problem

[P. Machanik: Approaches to Addressing the Memory Wall, TR Nov. 2002, U. Brisbane]

Clock speed

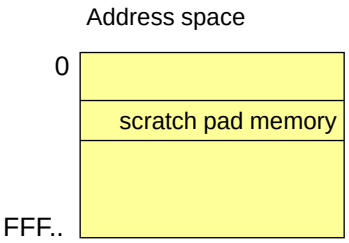


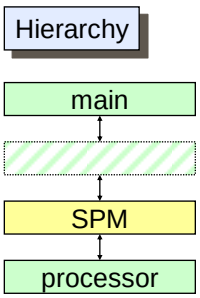
Parallel performance



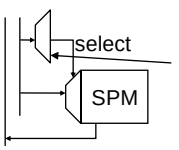
Hierarchical memories using scratch pad memories (SPM)

SPM is a small, physically separate memory mapped into the address space



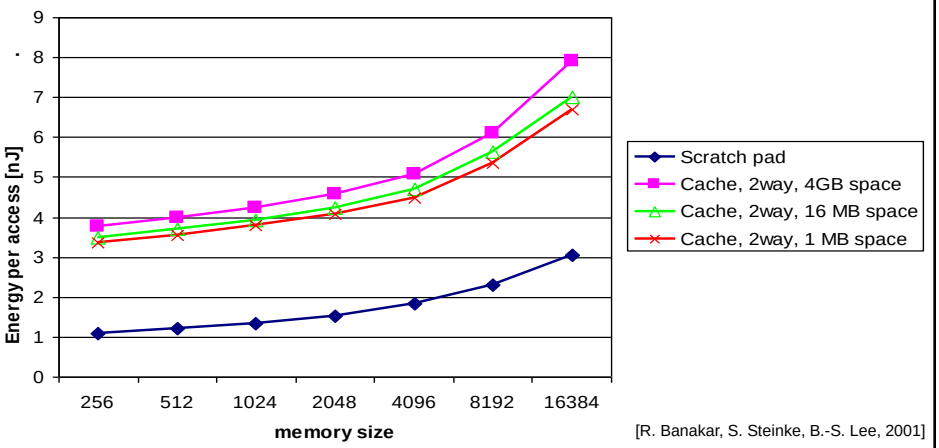


no tag memory



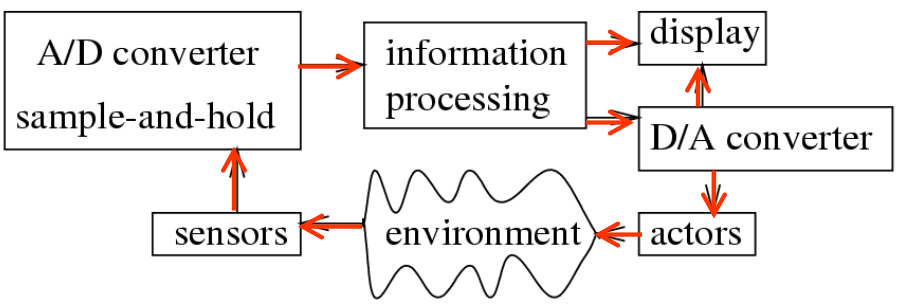
Selection is by an appropriate address decoder (simple!)

Energy consumption per memory access



[R. Banakar, S. Steinke, B.-S. Lee, 2001]

Communication

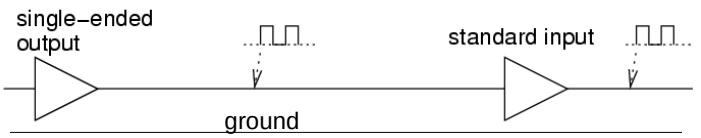


Communication requirements

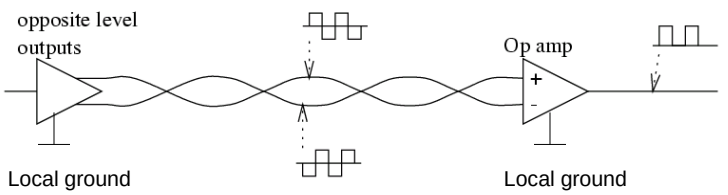
- Real-time behavior
- Efficient, economical
  (e.g. centralized power supply)
- Appropriate bandwidth and communication delay
- Robustness
- Fault tolerance
- Diagnosability
- Maintainability
- Security
- Safety

Basic techniques: Electrical robustness

- Single-ended vs. differential signals



Voltage at input of Op-Amp positive → '1'; otherwise → '0'



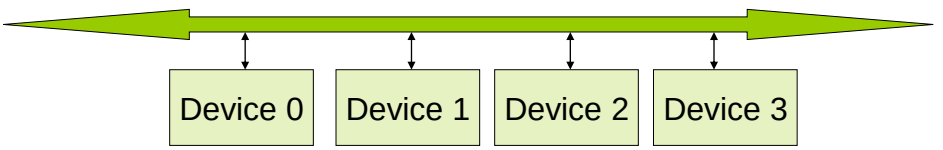
Combined with twisted pairs; Most noise added to both wires.

Evaluation

- **Advantages:**
  - Subtraction removes most of the noise
  - Changes of voltage levels have no effect
  - Reduced importance of ground wiring
  - Higher speed
- **Disadvantages:**
  - Requires negative voltages
  - Increased number of wires and connectors
- **Applications:**
  - USB, FireWire, ISDN
  - Ethernet (STP/UTP CAT 5/6 cables)
  - differential SCSI
  - High-quality analog audio signals (XLR)

Priority-based arbitration of communication media

For example, consider a bus



- Bus arbitration (allocation) is frequently priority-based

☞ Communication delay depends on communication traffic of other partners

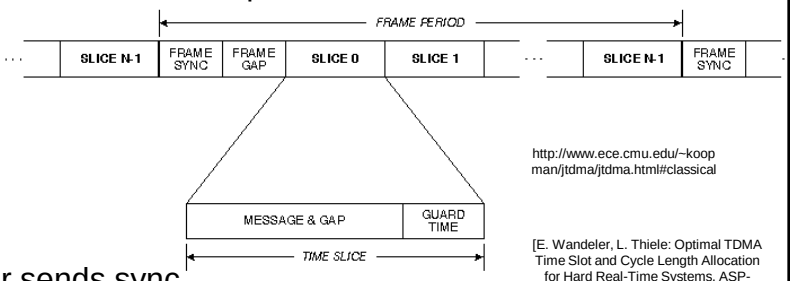
☞ No tight real-time guarantees, except for highest priority partner

Ethernet

- Carrier-sense multiple-access/collision-**detection** (CSMA/C**D**, Standard Ethernet): no guaranteed response time.
- Alternatives:
  - token rings, token busses
  - Carrier-sense multiple-access/collision-**avoidance** (CSMA/C**A**)
    - WLAN techniques with request preceding transmission
    - Each partner gets an ID (priority).
      After bus transfer: partners try setting their ID on the bus;
      Partners detecting higher ID disconnect themselves. Highest priority partner gets guaranteed response time; others only if they are given a chance.

Time division multiple access (TDMA) busses

- Each communication partner is assigned a fixed time slot. Example:



http://www.ece.cmu.edu/~koopman/jtdma/jtdma.html#classical

[E. Wandeler, L. Thiele: Optimal TDMA Time Slot and Cycle Length Allocation for Hard Real-Time Systems, ASP-DAC, 2006]

- Master sends sync
- Some waiting time
- Each slave transmits in its time slot
- **TDMA resources have a deterministic timing behavior**
- **TDMA provides QoS guarantees in networks on chips**